



### Features

- ◆ **High-speed address/chip select time**
  - Military: 25/35/45/55/70/85/100ns (max.)
  - Industrial: 25/35ns (max.)
  - Commercial: 20/25/35ns (max.) low power only
- ◆ **Low-power operation**
- ◆ **Battery Backup operation – 2V data retention**
- ◆ **Produced with advanced high-performance CMOS technology**
- ◆ **Input and output directly TTL-compatible**
- ◆ **Available in standard 28-pin (300 or 600 mil) ceramic DIP, 28-pin (600 mil) plastic DIP, 28-pin (300 mil) SOJ and 32-pin LCC**
- ◆ **Military product compliant to MIL-STD-883, Class B**

### Description

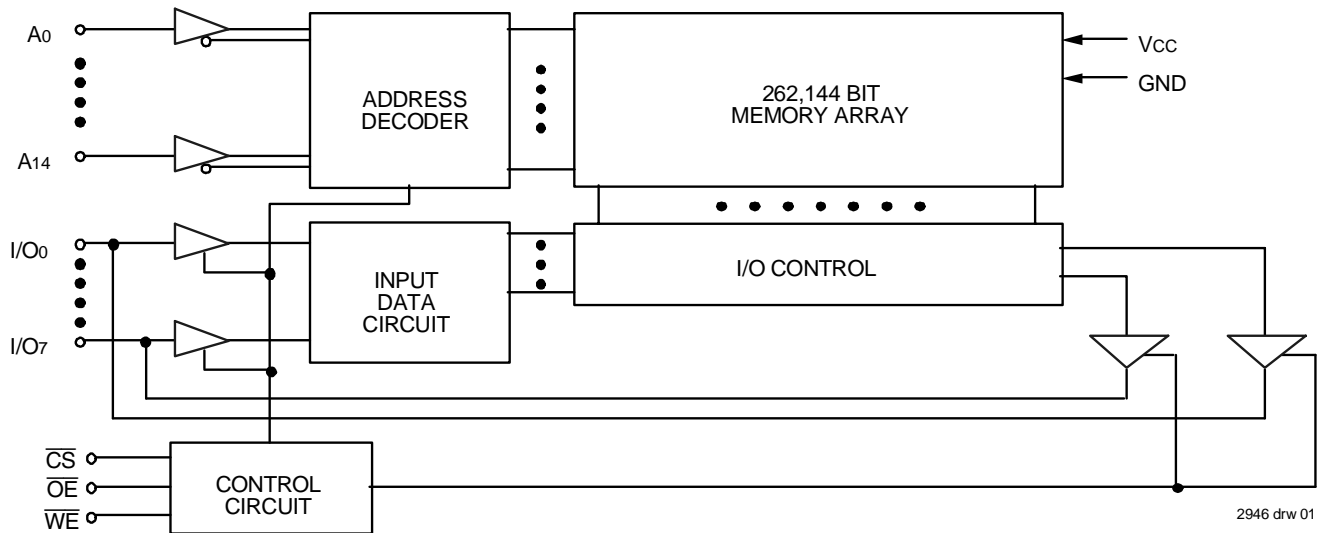
The IDT 71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When  $\overline{CS}$  goes HIGH, the circuit will automatically go to and remain in, a low-power standby mode as long as  $\overline{CS}$  remains HIGH. In the full standby mode, the low-power device consumes less than 15 $\mu$ W, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5 $\mu$ W when operating off a 2V battery.

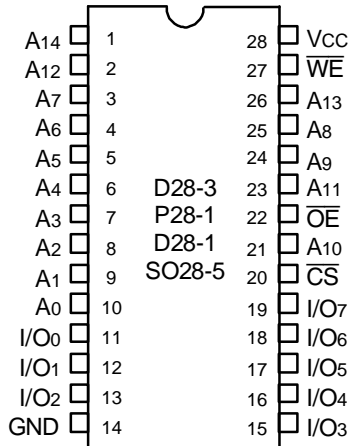
The IDT71256 is packaged in a 28-pin (300 or 600 mil) ceramic DIP, a 28-pin 300 mil SOJ, a 28-pin (600 mil) plastic DIP, and a 32-pin LCC providing high board level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### Functional Block Diagram

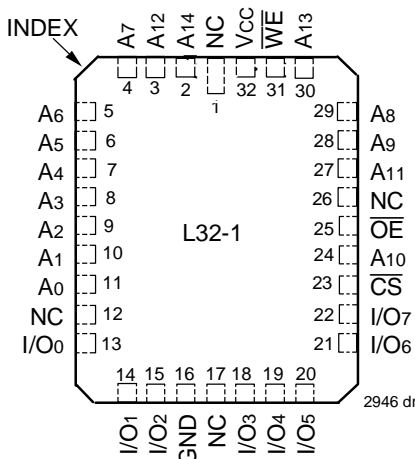


## Pin Configurations



2946 drw 02

DIP/SOJ  
Top View



2946 drw 03

32-Pin LCC  
Top View

## Pin Descriptions

Name	Description
A <sub>0</sub> - A <sub>14</sub>	Address Inputs
I/O <sub>0</sub> - I/O <sub>7</sub>	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V <sub>CC</sub>	Power

2946 tbl 01

## Truth Table<sup>(1)</sup>

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (I <sub>SB</sub> )
X	V <sub>HC</sub>	X	High-Z	Standby (I <sub>SB1</sub> )
H	L	H	High-Z	Output Disabled
H	L	L	DOUT	Read Data
L	L	X	DIN	Write Data

2946 tbl 02

### NOTE:

1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Mil.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-40 to +85	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	50	mA

2946 tbl 03

### NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	11	pF
C <sub>VO</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	11	pF

2946 tbl 04

### NOTE:

1. This parameter is determined by device characterization, but is not production tested.

### Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-40°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2946 tbl 05

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

2946 tbl 06

**NOTE:**

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.

### DC Electrical Characteristics<sup>(1,2)</sup> (V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

Symbol	Parameter	Power	71256S/L20		71256S/L25		71256S/L35		71256S/L45		Unit
			Com'l. & Ind	Mil.	Com'l. & Ind	Mil.	Com'l. & Ind	Mil.	Com'l.	Mil.	
ICC	Dynamic Operating Current CS ≤ V <sub>IL</sub> , Outputs Open V <sub>CC</sub> = Max., f <sub>MAX</sub> <sup>(2)</sup>	S	—	—	—	150	—	140	—	135	mA
		L	135	—	125	130	115	120	—	115	
ISB	Standby Power Supply Current (TTL Level), CS ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(2)</sup>	S	—	—	—	20	—	20	—	20	mA
		L	3	—	3	3	3	3	—	3	
ISB1	Full Standby Power Supply Current (CMOS Level), CS ≥ V <sub>HC</sub> , V <sub>CC</sub> = Max., f = 0	S	—	—	—	20	—	20	—	20	mA
		L	0.6	—	0.6	1.5	0.6	1.5	—	1.5	

2946 tbl 07

Symbol	Parameter	Power	71256S/L55	71256S/L70	71256S/L85	71256S/L100	Unit
			Mil.	Mil.	Mil.	Mil.	
ICC	Dynamic Operating Current CS ≤ V <sub>IL</sub> , Outputs Open V <sub>CC</sub> = Max., f <sub>MAX</sub> <sup>(2)</sup>	S	135	135	135	135	mA
		L	115	115	115	115	
ISB	Standby Power Supply Current (TTL Level), CS ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(2)</sup>	S	20	20	20	20	mA
		L	3	3	3	3	
ISB1	Full Standby Power Supply Current (CMOS Level), CS ≥ V <sub>HC</sub> , V <sub>CC</sub> = Max., f = 0	S	20	20	20	20	mA
		L	1.5	1.5	1.5	1.5	

2946 tbl 08

**NOTES:**

- All values are maximum guaranteed values.
- f<sub>MAX</sub> = 1/TRC, all address inputs are cycling at f<sub>MAX</sub>; f = 0 means no address pins are cycling.

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 09

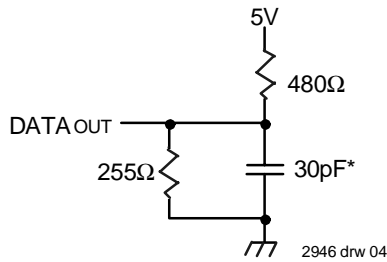


Figure 1. AC Test Load

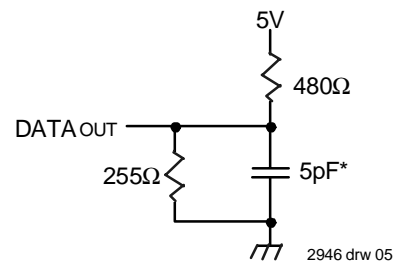


Figure 2. AC Test Load  
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

\*Includes scope and jig capacitances

## DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71256S			IDT71256L			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL. COM*L & IND.	—	—	10 5	—	—	5 2	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}$ = V <sub>H</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL. COM*L & IND.	—	—	10 5	—	—	5 2	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	—	0.4	—	—	0.4	V	
		I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	—	—	0.5	—	—	0.5		
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	—	2.4	—	—	V	

2946 tbl 10

## Data Retention Characteristics Over All Temperature Ranges

(L Version Only) (V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

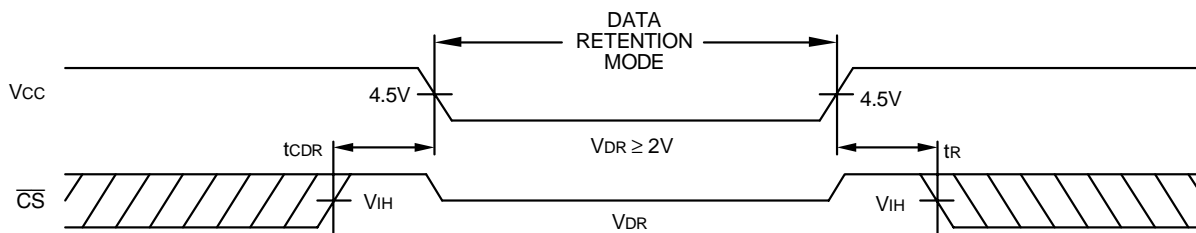
Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup> V <sub>CC</sub> @		Max. V <sub>CC</sub> @		Unit
				2.0V	3.0V	2.0V	3.0V	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	—	2.0	—	—	—	—	V
I <sub>CDR</sub>	Data Retention Current	MIL. COM*L & IND.	—	—	—	500 120	800 200	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$	0	—	—	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	—	—	ns

2946 tbl 11

### NOTES:

1. T<sub>A</sub> = +25°C.
2. t<sub>RC</sub> = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

## Low Vcc Data Retention Waveform



2946 drw 06

## AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256L20 <sup>(1)</sup>		71256S25 71256L25		71256S35 71256L35		71256S45 <sup>(3)</sup> 71256L45 <sup>(3)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	35	—	45	ns
t <sub>ACS</sub>	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	—	10	—	11	—	15	—	20	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	10	—	11	—	15	—	20	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable to Output in Low-Z	2	—	2	—	2	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Disable to Output in High-Z	2	8	2	10	2	15	—	20	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	15	—	20	—	30	—	40	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	15	—	20	—	30	—	40	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	15	—	20	—	30	—	35	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data to Write Time Overlap	11	—	13	—	15	—	20	—	ns
t <sub>WHZ</sub> <sup>(2)</sup>	Write Enable to Output in High-Z	—	10	—	11	—	15	—	20	ns
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(2)</sup>	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

2946 tbl 12

### NOTES:

- 0° to +70°C temperature range only.
- This parameter is guaranteed by device characterization, but is not production tested.
- 55°C to +125°C temperature range only.

AC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, Military Temperature Ranges)

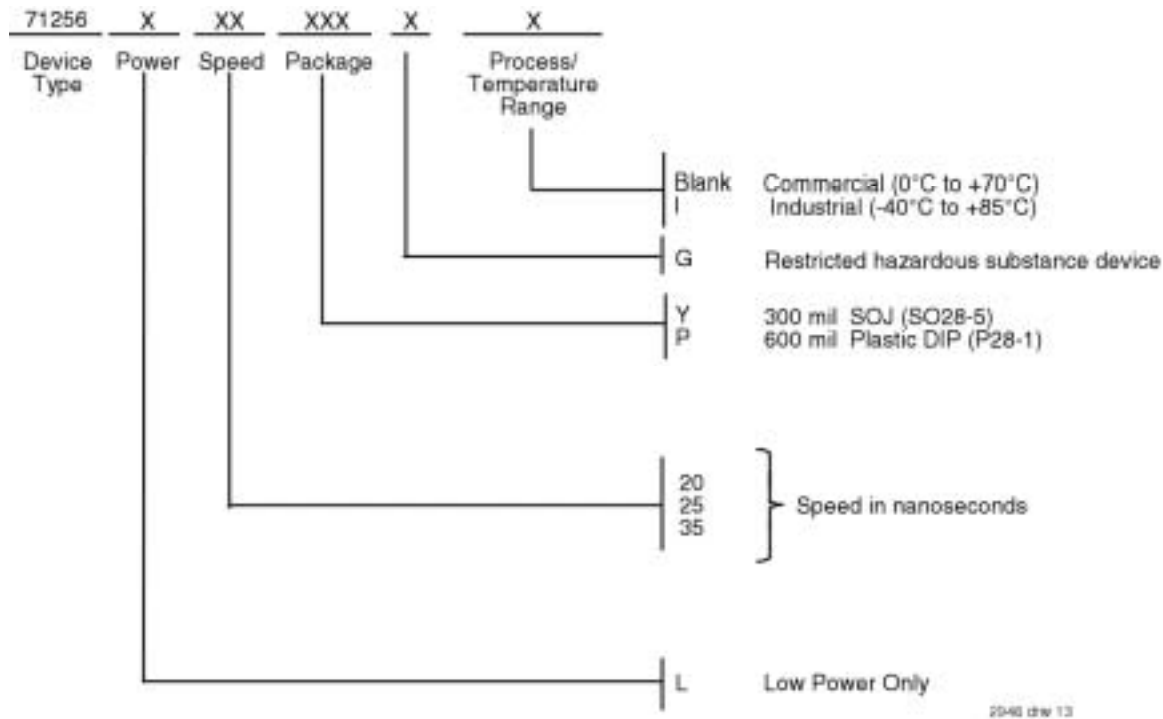
Symbol	Parameter	71256S55 <sup>(1)</sup> 71256L55 <sup>(1)</sup>		71256S70 <sup>(1)</sup> 71256L70 <sup>(1)</sup>		71256S85 <sup>(1)</sup> 71256L85 <sup>(1)</sup>		71256S100 <sup>(1)</sup> 71256L100 <sup>(1)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	—	85	—	100	ns
t <sub>ACS</sub>	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	—	25	—	30	—	35	—	40	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Disable to Output in High-Z	0	25	0	30	—	35	—	40	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	50	—	60	—	70	—	80	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	50	—	60	—	70	—	80	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	40	—	45	—	50	—	55	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
t <sub>WHZ</sub> <sup>(2)</sup>	Write Enable to Output in High-Z	—	25	—	30	—	35	—	40	ns
t <sub>DH</sub>	Data Hold from Write Time ( $\overline{WE}$ )	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(2)</sup>	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

2946 tbl 13

NOTES:

1. -55° to +125°C temperature range only.
2. This parameter is guaranteed by device characterization, but is not production tested.

### Ordering Information — Commercial & Industrial



### Ordering Information — Military

